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14. ABSTRACT

The goals of this project were to develop the technologies necessary to implement a new, non-contacting infrared sensing element. As described in our proposal, the sensing element is to be suspended in tension with electrostatic forces within a pixel cavity. The creation of this structure has required the development of a number of MEMS fabrication techniques. We have also developed new circuit topologies to the novel sensing structure.

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Uncooled Infrared Detector Arrays with Electrostatically Levitated Sensing Elements

Michael Reed and Travis Blalock

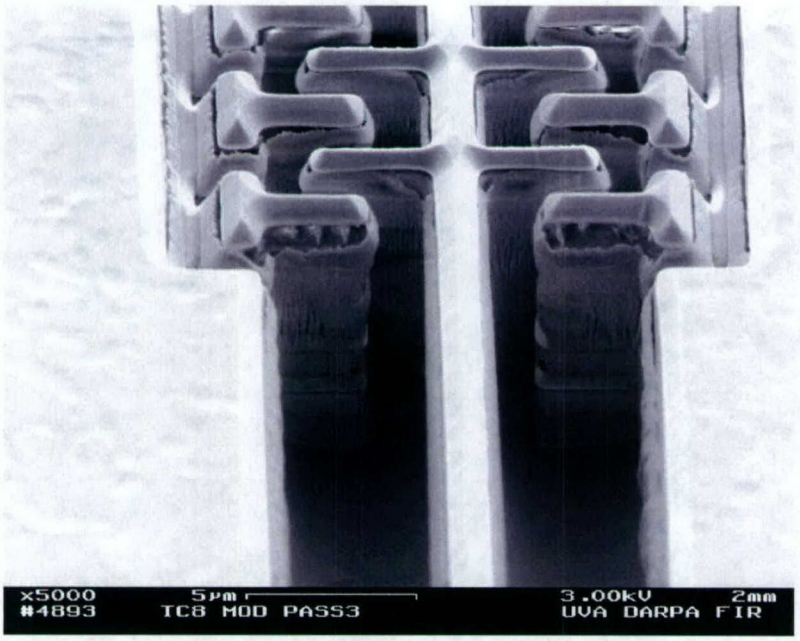
The goals of this project were to develop the technologies necessary to implement a new, non-contacting infrared sensing element. As described in our proposal, the sensing element is to be suspended in tension with electrostatic forces within a pixel cavity. The creation of this structure has required the development of a number of MEMS fabrication techniques. We have also developed new circuit topologies to interface to the novel sensing structure.

The circuit work focused on two readout methods. The first is a fully non-contacting capacitive readout method. After readout, the sensor is moved in contact with the substrate to quench the detector before the next thermal integration cycle. We also developed a circuit to perform a contacting readout. The readout is performed at the beginning of the quench cycle and must be performed rapidly to acquire the signal before the detector is quenched. Results from both of these efforts are described in the attached papers[1,2].

A patent application [3] covering the novel aspects of is in process. The claims have been allowed and the patent should issue soon.

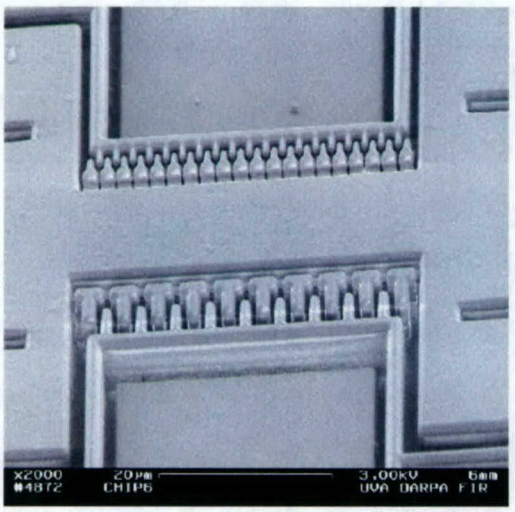
In the process development area, our objectives included several major challenges: engineering a reactive ion etching process for composite metal/oxide microstructures with minimum dimensions of 0.5 microns and aspect ratios exceeding 15:1; development of a refill/planarization process utilizing an organic sacrificial material which could be preferentially removed without affecting other structural or electronically active layers; and development of sputtered insulator and IR sensitive material deposition processes compatible with commercially fabricated CMOS integrated circuits. Substantial progress was achieved in all of these areas.

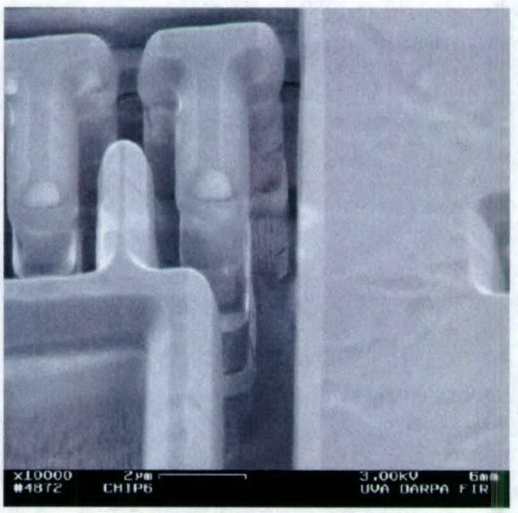
Chief among the engineering challenges was reactive ion etching of the insulating oxides in the CMOS multilevel-metal layers deposited during the IC manufacture. Because the deposition process was not under our control, the etch procedure had to be sufficiently robust to account for manufacturing variations. State-of-the-art etch processes existing at the outset of the program had been developed for three-level-metal interconnect schemes, with a total height of approximately five microns, and a minimum microstructure gap of two microns; thus the etched channel aspect ratio demonstrated at the time was approximately 2.5:1. The electrostatic force requirements of this application required a process using five metal layers, with a total thickness of approximately eight microns. This alone put significant importance on the ability of the etch to drill down through a significant thickness of oxide without undue erosion of the mask, the top level metal layer whose properties were likewise set by the IC manufacturer. See figure below.



Initial estimates of the required microstructure gap was approximately one micron; more detailed investigations revealed a narrower gap of approximately 0.5 microns was needed. Thus, the aspect ratio of the etched gap was increased from the existing 2.5:1 to over 15:1, a fourfold increase.

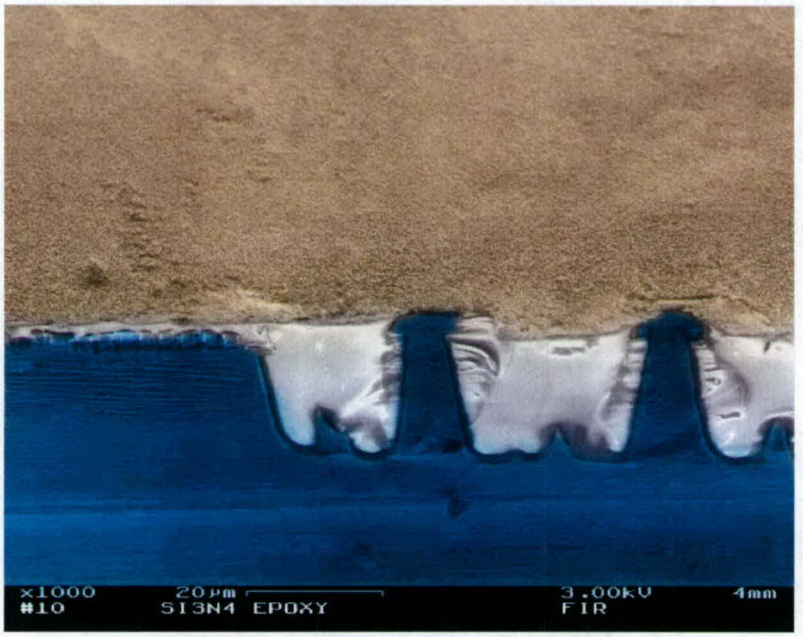
Despite these stringent requirements on etch performance, an etch recipe capable of high aspect ratio microstructure fabrication was developed. The left micrograph below illustrates interdigitated finger structures with gap spacing of 0.46 (top) and 0.92 (bottom) microns. A close-up of the the latter is shown in the right micrograph. These illustrate robust, intact laminated microstructures with no out-of-plane deflection, perfectly straight sidewalls, acceptable top mask erosion, and a lack of etch stringers and etch "grass" often encountered in minimum geometry reactive ion etching.





After experimenting with various organic materials including waxes, polymers, and resists, an excellent material for refilling the reactively ion etched microstructures was selected: a low viscosity thermosetting epoxy with a zero differential coefficient of thermal expansion (DCTE) relative to silicon, Epo-Tek 330. This material, originally designed for bonding fiber optic components, cures without cracking or outgassing, and was found to be compatible with the microelectronic components and microstructure post-processing steps. Most importantly, the zero DCTE properties ensured minimal induced mechanical stress which other materials introduced into the substrate and microstructures.

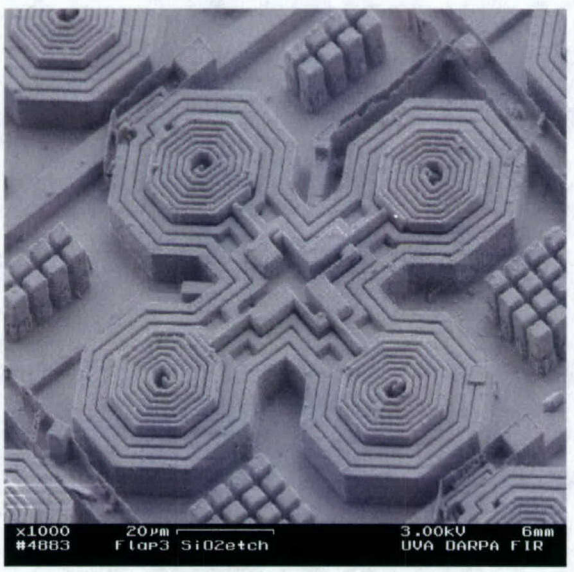
Related to the refill process was a technique developed for planarizing the sacrificial material. This was necessary owing to subsequent deposition of insulating and IR sensitive thin films. Our initial plan was to employ optically flat glass substrates in contact with the epoxy, followed by a sacrificial etch of the glass. This proved to be problematic as the hydrofluoric acid, required for dissolution of the glass, would also attack the insulating oxide in the composite microstructures.The long time required for glass etching, combined with large manufacturing tolerances in the glass thickness which translated into variable etch times precluded the success of this approach. An alternative method utilizing optically flat crystals of salt, NaCl, was developed. Although somewhat fragile, the salt crystals were successfully employed to planarize the epoxy film; dissolution was performed in warm water rather than hydrofluoric acid, which would occur in seconds rather than hours. The micrograph below illustrates micron-scale gaps filled and planarized using the process developed under this program.



Processes for sputtering thin films of silicon nitride and IR sensitive silicon films were also developed. A common difficulty with sputtered insulating films is a high pinhole density, which

leads to electrical shorts between the conducting films under and on top of the insulator. (The micrograph shows a pinhole typical of those encountered with insulator sputtering.) Pinhole density was reduced to acceptable levels by performing the deposition at an elevated temperature.

The technology developed here was applied to a new class of acoustic transducer, a magnetically coupled sensor/actuator pair designed for use in a phased array ultrasound imager. These transducers have significant advantages over piezoelectric and electrostatic approaches; chief among these are a low characteristic impedance suitable for interfacing with low-power integrated circuits. A micrograph of a prototype structure fabricated using our processes is shown below.



References:

S. N. Chanderkar, M. L. Reed, and T. N. Blalock, "CMOS Non-Contacting Readout Circuits for Infrared Sensors," Proc. of the IASTED International Conference on Circuits, Signals, and Systems, May 19-21, 2003, pp. 368-372.

A. Anumula, M. L. Reed, and T. N. Blalock, "CMOS Baseline Subtraction Readout Circuit for Infrared Sensors," Proc. of the IASTED International Conference on Circuits, Signals, and Systems, May 19-21, 2003, pp. 362-367.

M.L. Reed and T. N. Blalock, "Levitated Infrared Sensors," US Application No. 10/204,676.

Nicholas Jankowski (M.S., 2002). Thesis: "Reactive Ion Etch Development for the Fabrication of High-Aspect-Ratio Microelectromechanical Systems via 0.25 micron CMOS Post-Processing."

Arvind Anumula (M.S., May 2003). Thesis: "CMOS Low Noise Baseline Subtraction Readout Circuit for Infrared Bolometers."

Sheetal Chanderkar (M.S., May 2003). Thesis: "Non-Contacting CMOS Readout Circuit for an Array of Electrostatically Levitated Infrared Sensors."

Appendix (circuit papers):

CMOS BASELINE SUBTRACTION READOUT CIRCUIT FOR INFRARED SENSORS

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ABSTRACT

This paper discusses a new CMOS baseline and offset correction scheme for infrared bolometer focal plane arrays. The readout circuit allows for pixel level baseline subtraction eliminating most sources of per-pixel fixed pattern error and conside rably reducing imaging system complexity and overhead. The readout scheme includes a regulated constant voltage detector interface, a switched current offset correction circuit, and an integrator. Simulation results illustrate the high linearity and low noise of the readout circuit.

KEY WORDS

Bolometer, Offset Correction, Infrared, Switched Current Cell

Introduction

In thermal imaging, using uncooled rather than cooled infrared (IR) detector arrays offers the advantages of low cost, low weight, large spectral response, and long term operation. Among thermal IR detectors, integrated monolithic thin film uncooled bolometers offer advantages with respect to production, volume, yield and reliability [1]. Uncooled bolometers are IR detectors operating at room temperature. Their resistance changes following a temperature rise from the absorption of incident radiation. This resistance change serves as a measure of temperature of the object with respect to the surroundings.

Advances in Micro-Electro-Mechanical Systems (MEMS) technology have helped to create a new kind of bolometer that can be moved and brought into contact with the substrate [2]. This feature permits a new kind of readout scheme wherein the resistance of the detector quenched to the substrate serves as a baseline for measuring resistance change due to absorption of IR radiation. The detector is first allowed to absorb the incident radiation, and the resistance is measured and stored. The detector is then quenched to the substrate, followed again by readout, and this value is subtracted from the previous one to obtain a measure of the resistance change of the detector.

The resistance is found by applying a constant voltage across the detector. The resulting current is a measure of the resistance [4]. In this paper, a new baseline subtraction circuit is proposed. This scheme allows for pixel level offset correction, which eliminates most sources of per-element fixed pattern error.

The complete readout circuit includes a detector interface, a switched current memory offset-correction circuit, and a reset integrator. The pixel circuit includes a detector interface and offset correction circuit. The pixel size is 50 μm x 50 μm. The signal interfaces between the blocks are currents. Control of the individual circuits is implemented with a state-machine not discussed in this paper.

Constant Voltage Feedback Regulated Detector Interface

For illustration purposes, the whole readout scheme is represented in Fig.1.

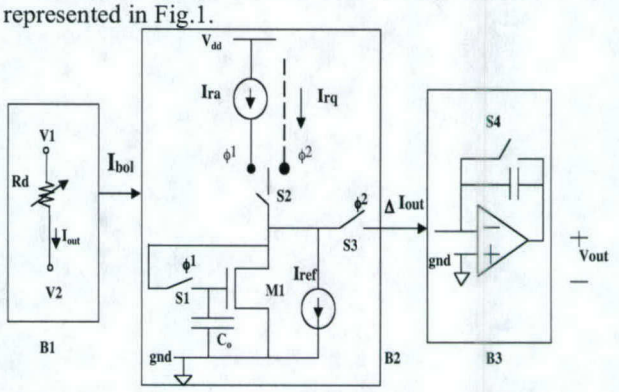

Figure 1: Simplified schematic of the readout circuits. Blocks B1 and B2 are included within each pixel circuit.

A low noise constant voltage circuit is interfaced to the bolometer as shown in block B1 of Fig.1. The Detector current, I_{bol}, which is a measure of detector resistance, is given to the block B2 as the input. The offset correction is achieved by a new IR detector readout method called switched current memory detector offset removal. During the post energy absorption phase ϕ1,

$$I_{bol} = I_{ra} = \frac{V_{bias}}{R_q + \Delta R_{heat}} \quad (1)$$

where R_q is the detector resistance when quenched, and ΔR_{heat} is the resistance change due to a temperature rise of the detector following the absorption of the IR radiation.

Switch S2 is closed during this phase, allowing I_{ra} to be stored on the gate-source capacitor of the diode-connected MOSFET M1. The detector is then quenched to the substrate temperature via a movable MEMS structure.
In the post quench phase, $\phi 2$, a readout is performed, where

$$I_{bol} = I_{rq} = \frac{V_{bias}}{R_q} \qquad (2)$$

and switch S3 is opened so that a subtraction between I_{rq} and stored I_{ra},is performed. The difference current, ΔI_{out},

$$\Delta I_{out} = I_{ra} - I_{rq} \approx \frac{V_{bias} \times \Delta R_{heat}}{R_q^{\,2}}, \qquad (3)$$

is a measure of resistance change, arising from this subtraction is then integrated over the reset integrator as shown in block B3.
Blocks 1 and 2 are implemented as shown in Fig 2. This is done to satisfy low noise, low area, and low power requirements for a pixel circuit.
This circuit will be integrated with an on-chip sensor in every pixel, and the reset integrator implemented in a column fashion.

Circuit Design Issues

The resolution of the baseline subtraction operation is improved by the addition of I_{ref}[6] to reduce the sensitivity of ΔI_{out} to the V_{gs} of M1. Because the majority of the current is carried by I_{ref}, charge injection at the gate of M1 gives rise to only a small error as a percentage of the total current. The sensitivity is also reduced by designing M1 with a low transconductance.

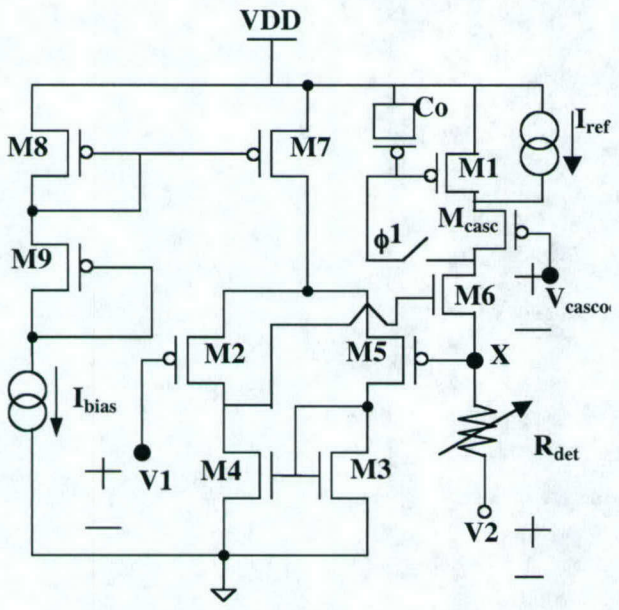

Figure 2. Pixel circuit. This shows both regulated voltage source and offset correction circuit. Negative feedback ensures a voltage drop of (V1-V2) across the detector.

Accuracy in the subtraction of currents is affected by several non-idealities in the circuit. These include the charge injection of switch S1, channel length modulation of M1, gate leakage current of M1 during the storage period, and noise contributed by several MOSFETs in the circuit.
The charge injection of switch S1 changes V_{gs} and the value of the stored current, I_{ra}. The effect of charge injection is suppressed by the addition of dummy switches with complementary clocking on either sides of S1, maximizing the capacitance at the gate of M1 [7], and the addition of I_{ref} as mentioned earlier.
Another source of error is due to the channel length modulation of M1. The finite output impedance of M1 is a source of error as the drain Voltage ($V_{ds,M1}$) is different in two readout phases. This effect is minimized by keeping the output integrator bias close to the V_{ds} or V_{gs} of M1 in phase $\phi 1$. Also a cascode transistor $M_{cascode}$ is introduced to reduce the variation of $V_{ds,M1}$.
Gate leakage current of M1 introduces an error ΔI_{err}, in the stored current value I_{ra} which can be approximately quantified as [6]

$$\Delta I_{err} = \frac{g_m * I_{leak} * \Delta t}{C_o} \qquad (4)$$

where I_{leak} is the leakage current and Δt is the time for which I_{ra} is stored. For nominal values of $I_{leak}=10^{-15}$ A (0.35μm process) and Δt=0.5ms, ΔI_{err} is approximately 0.25 pA which is negligible compared to $(\Delta I_{out})_{min}$.

Noise Analysis

Noise in the readout circuit and in the resistive sensor limit the accuracy of ΔI_{out}. This places a lower bound on the smallest measurable change in the resistance of the sensor and hence the minimum possible temperature change that can be detected. Therefore, a thorough analysis of the contribution of different noise sources is performed.
Noise in the circuit is due to thermal and 1/f noise generated by several CMOS transistors. As with other switched data circuits, the output noise current contains both sampled and direct noise components [8]. Previously, 1/f noise was not a significant factor in calculating the sampled noise components [9]. However, due to high 1/f corner frequencies observed in present day sub-micron processes [10] and due to low sampling frequencies in this application, 1/f noise can be a significant factor. Hence in this paper, a detailed analysis of the contribution of 1/f noise on sampled noise is presented. Analysis of thermal noise is similar to the analysis described below and is discussed in detail in [9].

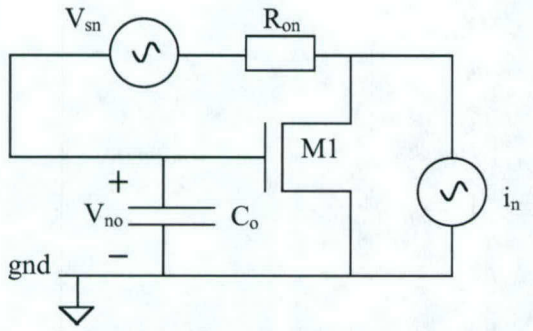

Figure 3. Correction circuit during the post absorb readout or sampling phase.

Figure 3 shows the equivalent circuit during the sampling operation. Noise is primarily due to M1 and switch S1 shown in Fig. 3. The effect of other elements in the circuit is combined into the noise current source of M1 (i_n). Dominant contribution to the noise in ΔI_{out} is by i_n since it adds directly to ΔI_{out}. The switch noise voltage V_{sn} appears across the gate–drain terminals and hence has lesser impact on the overall noise in ΔI_{out}.

Considering noise contributed by M1, the two-sided power spectral density (PSD) of the voltage across the capacitor due to the noise current of M1 is given by,

$$S_{v,n}(f) = \frac{1}{1+(f/f_o)^2} * \frac{S_{i,n}(f)}{g_{m1}^{\ 2}} \quad V^2/Hz \qquad (5)$$

where,

$$S_{i,n}(f) = \frac{1}{2}\frac{K_F}{C_{ox}WL} * \frac{1}{f} * g_{m1}^{\ 2} \quad A^2/Hz \qquad (6)$$

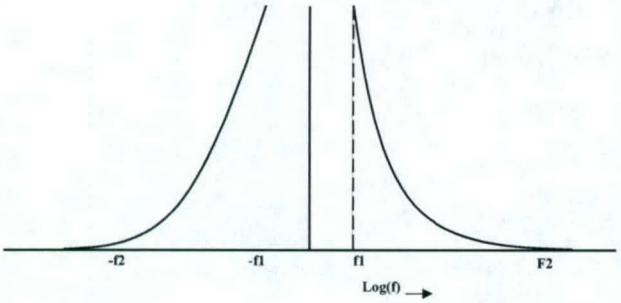

Figure 4. Power spectral density of voltage(Vn) across the capacitor(C_o).

and f_o is the pole frequency due to the low pass filtering action of the capacitor C_o. The transconductance of M1 is denoted by g_{m1}. The frequency content below f_1 can be treated as DC offset removed by the offset correction technique. Hence, it has been neglected and the resulting PSD of V_n is shown in Figure 4.By sampling the noise voltage at a frequency (f_s) much lower than the 1/f corner frequency, significant aliasing of the high frequency components is observed. As shown in [8], the PSD of the sample-and-held noise voltage $S^{S/H}{}_{v,n}(f)$ is related to $S_{v,n}(f)$ as follows:

$$S^{S/H}{}_{v,n} = \left(\frac{\tau}{T}\right)^2 \left(\frac{\sin\pi\tau f}{\pi\tau f}\right)^2 \sum_{k=-\infty}^{\infty} S_{v,n}(f - k * f_s) \quad (7)$$

where τ/T is the fraction of the sampling time interval($T=1/f_s$) for which the sample is held on the capacitor C_o.

Calculating the summation is tedious and provides little insight from a design perspective. Instead, an approximate solution can be found by making the following assumptions:

$$f_1 \approx f_s / 20, \text{ and}$$

$$f_s << Min(f_o, f_2),$$

where f_2 is the 1/f corner frequency. Since the circuit is meant for imaging applications, the sampling frequency is low(in KHz range) and hence these assumptions are valid for this case.

Using the above assumptions, Figure 5 indicates that the summation can be approximated by a constant value $S(f_1)$. This is obtained by assuming that for frequencies close to f_1 and for frequencies a distance f_1 away from multiples of f_s, the tails of the other aliased components do not add much to the existing noise PSD value.

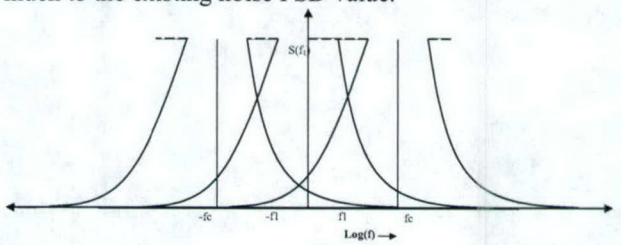

Figure 5. Summation of aliased components of 1/f noise of Vn.

The baseline correction cancels out the noise at DC and at multiple frequencies of f_s. The above approximation breaks down when $f_1 << fs$, as the summation of the PSD results tend to appear concave. The approximation is also not valid when fs is of the same magnitude as f1.

Therefore, $S^{S/H}{}_{v,n}(f)$ can be written as

$$S^{S/H}{}_{v,n} = \left(\frac{\tau}{T}\right)^2 \left(\frac{\sin\pi\tau f}{\pi\tau f}\right)^2 * S_{v,n}(f_1) \qquad (8)$$

Combining both the direct and sampled flicker noise, and assuming uncorrelated sources, the total flicker noise contribution for the output noise current is given by

$$S^{1/f}{}_{i,n}(f) = S^{S/H}v,n(f) * g_{m1}^{\ 2} + S_{i,n}(f) * m, \quad (9)$$

where mT is the fraction of time for which the output current is connected to the integrator.

Similarly, the thermal component of the output noise current is found as in [3],

$$S^{T}{}_{i,n}(f) = S_{i,n}(f) + S^{S/H}{}_{i,n}(f), \qquad (10)$$

where $S_{i,n}(f)$, the direct thermal noise component, is given by

$$S_{i,n}(f) = m * \frac{4KT * g_{m1}}{3}, \qquad (11)$$

and the sample-and-hold component is given by,

$$S^{S/H}{}_{i,n}(f) = \left(\frac{\tau}{T}\right)^2 \sin c^2(f\tau)\left(\frac{g_{m1}/2C_o}{f_s}\right)\left(\frac{4KTg_{m1}}{3}\right). \qquad (12)$$

Hence, the total noise is found by integrating over the band of interest. Using typical values of W/L=0.4/15, f_s=2 KHz, f_2= 200 KHz, and f_1=100 Hz, τ approaching 1, and g_{m1}=0.5 μA/V, the sampled flicker noise is 0.1 pA and the sampled thermal noise is 50pA. The contribution of direct noise sources is much lower and therefore not included. Traditional reset-integrators used in infrared imaging applications integrate the desired signal along with the baseline and offset signals. This limits the dynamic range of the output signal. By integrating only the difference current signal, this limitation is overcome. The reset integrator does not seriously affect the noise performance, as the noise voltage is developed across the gate-drain voltage of M1 during ϕ2.

Simulation Results and Discussion

The entire readout architecture with the feedback regulated constant voltage detector bias, baseline and offset correction circuit, and integrator has been simulated using the 0.35 μm TSMC design kit for Cadence. Figure 5 shows ΔI_{out} as a function of time for different resistance changes of the detector. Glitches observed in the waveform are due to the switching action in the circuit. Only three waveforms have been identified in Figure 6, for the sake of clarity. The discrepancy in the calculated values and the observed values can be explained by the non-idealities in the regulated voltage source which appears only as a gain error and can be corrected with post-processing. Figure 7 shows the variation of the change in integrator output voltage against resistance changes. The plot demonstrates the high linearity obtained through the detector baseline and offset correction circuit. Figure 8, shows the high linearity of ΔI in Fig. 3(b) vs. resistance change of the detector

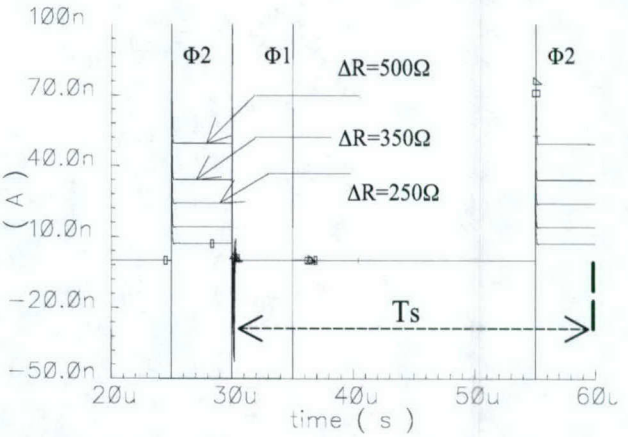

Figure 6. ΔI_{out} vs. time for different ΔR_{det}.

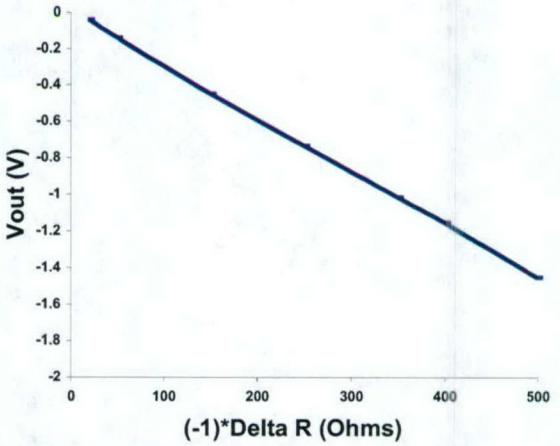

Figure 7. Integrator output voltage change (V_{out}) vs. resistance change (ΔR).

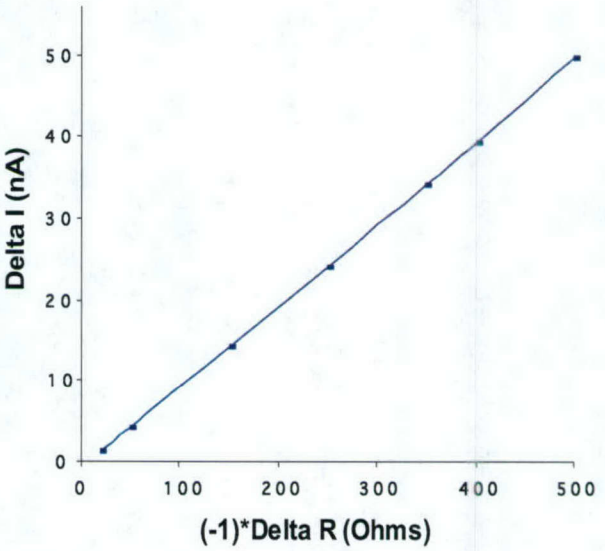

Figure 8. Difference current vs. resistance change.

In Figure 9, the layout of the pixel circuit along with the supporting structure for the MEMS temperature sensor is shown. Pixel size is 50 μm x 50 μm. Early results for a baseline subtraction readout technique which does pixel

level offset correction, have been presented. A chip with prototype readout circuits has been submitted for fabrication and future work will involve testing and characterization of the new circuits.

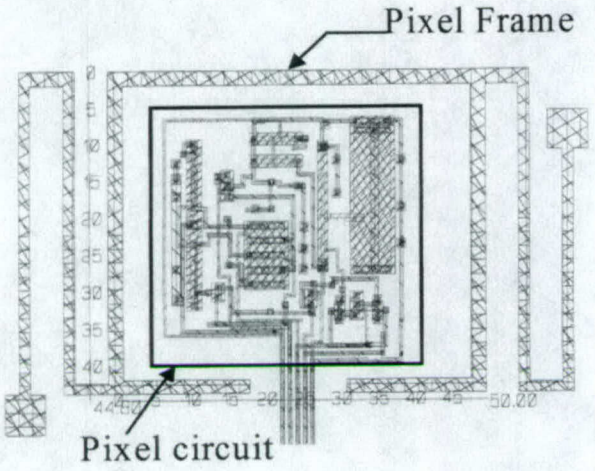

Figure 9. Layout of unit cell with pixel frame and readout circuit

References

[1] Ulf Ringh, Christer Jansson and Kevin Liddiard Readout Concept employing a novel on chip 16 bit ADC for smart IR focal plane arrays," in Proc. SPIE, Orlando, FL, Apr. 1996, pp. 99—110.

[2] M. L. Reed, T. N. Blalock, Levitated Infrared Sensor Apparatus and Method of Using the Same, US patent applied for, February 24, 2001;International patent applied for, February 26, 2001.

[3] Akio Tanaka and Shouhei Matsumoto, "Infrared Focal Plane array incorporating silicon IC process compatible Bolometer," IEEE Trans. Electron Devices, vol. 43, no. 11, Nov. 1996

[4] N. Bluzer and R. Stehlik, "Buffered direct injection of photocurrents into charge coupled devices," IEEE Trans. Electron Devices, vol. 25, no. 2, pp. 160–166, 1978.

[5] Tsung-Hsin Yu et al, "A New CMOS readout circuit for uncooled Infrared bolometric Focal Plane arrays," ISCAS 2000, Geneva, May 2000, vol. II, pp 493-496.

[6] H. J. Schouwenaars, D. W. J. Groeneveld, and H. A. H. Termeer. "A low-Power Stereo 16-bit CMOS D/A Converter fpr Digital Audio," IEEE J. of Solid-State Circuits, Vol. 23, pp. 1290-1297, December 1988.

[7] Eichenberger C, Guggenbuhl W. "On charge injection in analog MOS switches and dummy switch compensation techniques." IEEE Transactions on Circuits & Systems, vol.37, no.2, Feb. 1990, pp.256-64.

[8] R. Gregorian and G. C. Temes, Analog MOS Integrated Circuits for Signal Processing. New York: Wiley & Sons 1986, ch. 7, pp. 505-513

[9] S.J. Daubert and D. Vallancourt "Operation and analysis of current copier circuits." IEEE proceedings, Vol 137 April 1990, pp 109-115

[10] Razavi B, Design of Analog CMOS Integrated Circuits, Mc.Graw Hill, 2000.

NON-CONTACTING CMOS READOUT CIRCUIT FOR AN ARRAY OF ELECTROSTATICALLY LEVITATED INFRARED SENSORS

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ABSTRACT

This paper introduces a technique to accomplish readout of an infrared detector via capacitive coupling of an oscillator without direct DC contact between the sensor and electrodes. Avoiding direct physical contact between the infrared detector and the readout electrodes minimizes thermal conduction losses, providing a more accurate and sensitive measurement of the infrared power incident on the sensor. An analog CMOS voltage controlled oscillator with an oscillation frequency of 79 MHz and phase noise of –104 dBc/Hz @ 1 KHz offset is discussed and investigated as the non-contacting readout circuit.

KEY WORDS
Bolometer, CMOS, sensors, oscillator, phase noise

1. INTRODUCTION

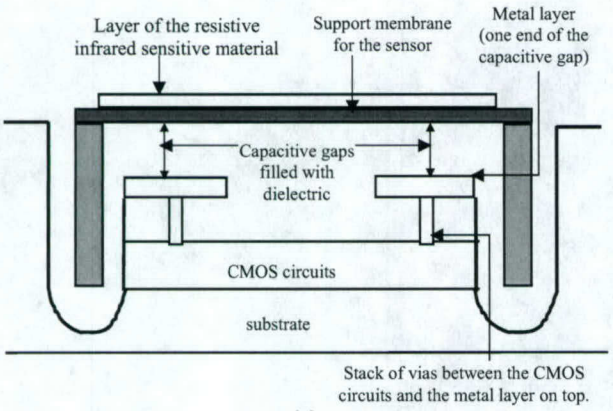
A microbolometer operates on the principle that infrared radiation incident on the surface of the infrared sensor causes a change in its temperature. This temperature change gives rise to a change in the sensor resistance proportionate to the temperature coefficient of resistance (TCR) of the sensor material. Thus, the change in the resistance of the sensor provides a useful measure of the incident infrared power.

Although in recent times, uncooled microbolometer arrays have seen tremendous progress with several state-of-the-art arrays exhibiting noise equivalent temperature differences (NETD) less than 100 mK, they have sensitivity limitations related to thermal conduction losses via contact legs between the detector and the readout circuitry. In order to overcome these limitations, a long wavelength infrared detector that is completely isolated from the substrate during energy absorption has been developed by combining MEMS fabrication techniques and basic electrostatic field concepts [1]. Since the detector element is levitated in a cavity above the substrate using electrostatic forces, the thermal losses are limited to radiation through the surrounding vacuum, improving the detector sensitivity.

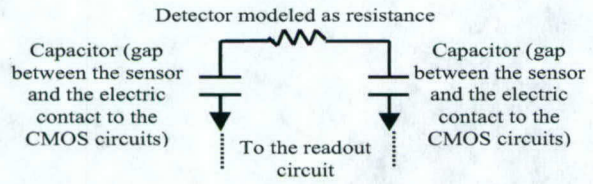
As seen in Fig. 1(a), in each pixel, the detector membrane is mounted on a frame that is kept in tension by electrostatic forces, centering the detector in-plane and perpendicular to the substrate. This results in effectively isolating the detector from the substrate by keeping it suspended in a cavity etched within the substrate. The detector platform on which the infrared sensitive film is deposited forms a part of a micro-electro-mechanical system (MEMS). The CMOS readout electronics are integrated with the sensor platform. The topmost layer of metal in the CMOS process is used to define the microstructures as well as to protect the CMOS circuitry from the etch processes used to define and release the microstructures. A retaining structure is used to maintain the position of the detector with respect to the substrate after the final release etch in case the array is subjected to unusually fast movements when power is not applied.

Readout of the detector requires sensing of the resistance change of the levitated sensor. In order to fully exploit the levitated sensor architecture, a non-contact readout scheme has been developed, which uses capacitive coupling instead of a DC contact with the suspended platform to sense the changes in sensor resistance. The advantages of this approach are:
1) The detector temperature is not disturbed by thermal conduction losses with the electrodes during readout.
2) It simplifies the detector platform fabrication by avoiding structures to accomplish direct DC contact with the detector.

Actual implementation of the capacitive coupling readout technique involves the use of a CRC series circuit formed by the electrode vacuum gaps and the detector resistance as shown in Fig. 1(b). The detector is the topmost layer consisting of a layer of infrared sensitive material (α-Si or vanadium oxide, VO_x) over a layer of silicon nitride.



(a)



(b)

Figure 1. (a) Cross-section of the detector coupled capacitively with the underlying CMOS circuits [1]. (b) A CRC model of the detector and its capacitive coupling.

2. DESCRIPTION AND ANALYSIS OF THE OSCILLATOR

In the proposed readout circuit, the CRC series circuit is used as the passive network that governs the output frequency in an oscillator. R_{mos}, a resistor implemented using a MOS transistor and C_{par} provide the required phase shift and biasing. Any change in the output frequency of the oscillator provides a direct indication of the change in the resistance of the detector and thus, the change in incident infrared power. The change in temperature caused by a change in the amount of infrared power incident on the sensor, is related to a change in the detector resistance by the following equation [2].

$$R_d - R_{do} = \dot{A} T R_{do} \acute{a} \qquad (1)$$

where $\alpha = 0.01\ K^{-1}$ (temperature coefficient of detector resistance), R_{do}=initial value of resistance, and ΔT= change in temperature. Typically, for the designed bolometer, the value of $(R_d - R_{do})$ is approximately 2Ω for a 10mK change in temperature and a detector resistance of $23K\Omega$.From Fig. 2,

$$Z_1 = R_d - 2jXc_d \qquad (2)$$

$$Z_2 = R_{mos} \,||\, -jXc_{par} \qquad (3)$$

$$\beta = \frac{v_f}{v_o} = \frac{Z_2}{Z_1 + Z_2} \qquad (4)$$

$$\beta = \frac{1}{\left(1 + \frac{2Xc_d}{Xc_{par}} + \frac{R_d}{R_{mos}}\right) + j\left(\frac{R_d}{Xc_{par}} - \frac{2Xc_d}{R_{mos}}\right)} \qquad (5)$$

Barkhausen's criteria for oscillation are:

1) The total loop gain for the differential amplifier and feedback should be unity,

$$|A(\omega)\|\beta(\omega)| = 1 \qquad (6)$$

where A is the transfer function of the amplifier, β is the transfer function of the passive feedback network and ωis the frequency of oscillation.

2) The phase shift around the amplifier and feedback loop should be an integer multiple of 2π.

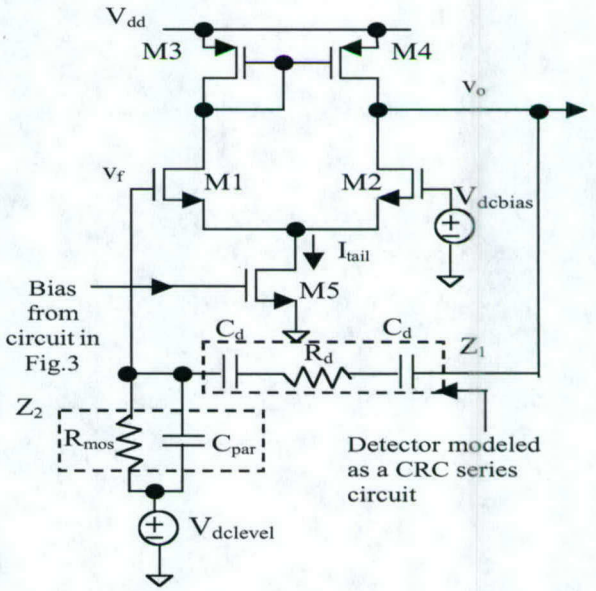


Figure 2. Oscillator with the CRC series circuit as the passive frequency selective network in the feedback loop of a differential amplifier.

Since the differential amplifier is used in non-inverting mode, in order to satisfy the second Barkhausen's criterion for oscillation, we have

$$\angle \hat{a} = -tan^{-1}\left(\frac{\frac{R_d}{Xc_{par}} - \frac{2Xc_d}{R_{mos}}}{1 + \frac{2Xc_d}{Xc_{par}} + \frac{R_d}{R_{mos}}}\right) = 0 \qquad (7)$$

Solving Eqn. (7), the frequency of oscillation in radians is given by

$$\grave{u} = \sqrt{\frac{2}{R_{mos} R_d C_{par} C_d}} \qquad (8)$$

From Eqn. (5), magnitude of the feedback factor is

$$|\beta(\omega)| = \frac{1}{\left(1 + \frac{2Xc_d}{Xc_{par}} + \frac{R_d}{R_{mos}}\right)} \qquad (9)$$

We also know that the open loop gain of the amplifier is

$$|A(j\omega)| = g_{M1,M2}(r_{oM2} \| r_{oM4}) \quad (10)$$

In order to satisfy the first Barkhausen's criterion for stable oscillations, we must ensure that

$$g_{M1,2}(r_{oM2} \| r_{oM4}) \geq 1 + \frac{2Xc_d}{Xc_{par}} + \frac{R_d}{R_{mos}} \quad (11)$$

where g_m is the transconductance and r_o is the output resistance of the specified transistors [3]. From Eqn (10), we know that since the gain of the amplifier depends on g_m, it also depends on I_{tail}. In order to minimize the power supply sensitivity of the tail current, a supply-insensitive self-biased or bootstrap current reference [4] shown in Fig.3 is used to derive the required tail current.

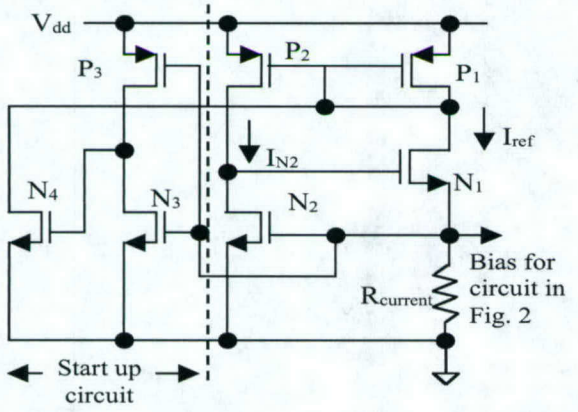


Figure 3. Self-biased current source along with start up circuit to set the tail current for the oscillator in Fig.2.

Except for the effects of finite output resistance of the transistors, the generated bias current is independent of the power supply.

$$I_{ref} = I_{N2} = \frac{V_{gsN2}}{R_{current}} = \frac{V_{th} + \sqrt{\frac{2I_{N2}L_{N2}}{\mu_n C_{ox} W_{N2}}}}{R_{current}} \quad (12)$$

Besides rejecting the supply voltage variation, the circuit also attenuates the small signal variations on the supply lines. The circuit has two stable operating points, one of which is a zero current state, and depending on past history, the circuit can stand in either of the two operating points. Hence, a start-up circuit is required to ensure that the circuit is not stuck in the zero current state.

For a more compact design and smaller pixel area, the biasing scheme can be shared by an entire row of pixels in the sensor array. Moreover, to reduce power consumption, a switch is inserted between the output of the bias circuit and the oscillator inside the pixel to effectively turn the oscillator off when its output is not being read out by disconnecting the bias circuit from the oscillator.

3. PHASE NOISE ANALYSIS OF THE OSCILLATOR

A practical oscillator has fluctuations in its amplitude and frequency. Noise (thermal, shot and flicker) and interference sources (substrate and supply noise) result in frequency instabilities. The spectrum of a practical oscillator has sidebands close to the frequency of oscillation and its harmonics [5]. These sidebands are referred to as phase noise and arise from narrow band phase modulation of the oscillator output (carrier) by noise. The random phase leads or lags induced by phase noise result in a deviation in the frequency of oscillation in order to compensate for the phase shifts and to maintain stable oscillations.

It is important to measure the frequency deviation caused by phase noise in the oscillator output in order to get an accurate measurement of a change in the detector resistance owing to a change in incident infrared power. From a frequency domain viewpoint, an oscillator's frequency instabilities are characterized in terms of the single sideband noise spectral density, $L(f_m)$, which is expressed in terms of dBc (decibels below carrier level) [5,6].

$$L(f_m) = 10\log\left[\frac{P_{SSB}(f_0 + f_m, 1\text{Hz})}{Pcarrier}\right] \quad (13)$$

where $P_{SSB}(f_0 + f_m, 1\text{Hz})$ is the single sideband power at an offset f_m from the oscillation frequency, f_o, in a 1Hz bandwidth, and $P_{carrier}$ is the total power under the oscillator spectrum. θ_{pk} is the peak phase deviation in radians (equal to the narrowband modulation index) given by f_{pk}/f_m, where, f_{pk} is the peak frequency deviation in Hz For small values of modulation index (<<1), as is the case with random phase noise, only the carrier and first upper and lower sidebands are significantly high in energy [6]. Hence, the ratio of the amplitude of either single sideband (V_{sb}) to that of the carrier (V_c) is

$$\frac{V_{sb}}{V_c} = \frac{\theta_{pk}}{2} \quad (14)$$

Thus from Eqn (13) and Eqn (14),

$$L(f_m) = 10\log\left(\frac{V_{sb}}{V_c}\right)^2 = 20\log\left(\frac{\theta_{pk}}{2}\right) = 20\log\left(\frac{f_{pk}}{2f_m}\right) \quad (15)$$

$$\therefore f_{pk} = 2f_m 10^{\frac{L(f_m)}{20}} \quad (16)$$

Using the value of L (f_m) obtained from simulation and from Eqn (16), we can determine the output frequency deviation (RMS) arising due to phase noise in the circuit and use it to calculate the NETD. These calculations yield a NETD of less than 20 mK for this detector circuit.

4. RESULTS

The simulation results are obtained after taking into account parasitic capacitances associated with the

transistors and the metal interconnects in the layout, as well as a bonding-pad capacitance of 15 pF at the output for the transient, periodic steady state, and periodic noise analyses. The typical values for the detector resistance and the capacitance between the detector and the electrode obtained through characterization of the bolometer are 23 KΩ and 18.5 fF, respectively.

The oscillator output is sinusoidal with a frequency of 79 MHz and a peak-to-peak value of 250 mV as shown in Fig. 4. The variations of the oscillator output frequency with respect to changes in detector resistance are plotted in Fig. 5.

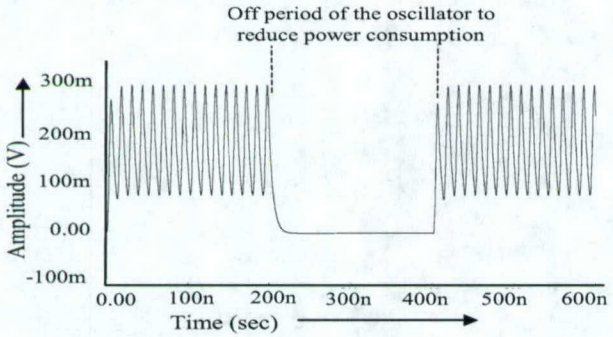


Figure 4. Oscillator output.

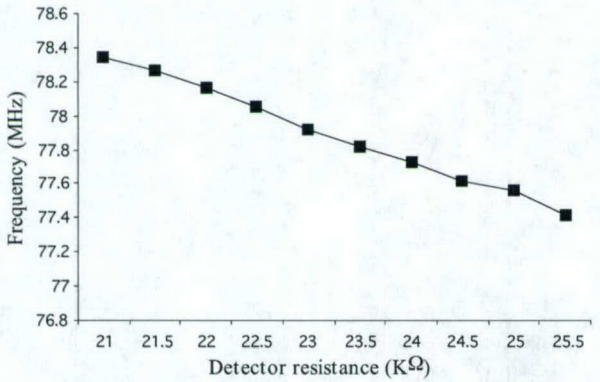


Figure 5. Change in the oscillation frequency (MHz) with respect to a percentage change in detector resistance.

The phase noise plot of the circuit is shown in Fig. 6. From Eqn (16) and the phase noise simulations, a rms frequency deviation of 282 Hz is observed in the band of interest around the fundamental oscillation frequency due to phase noise. Based on the parameters obtained from detector characterization and the value of total rms frequency deviation, a NETD of less than 20mK is calculated.

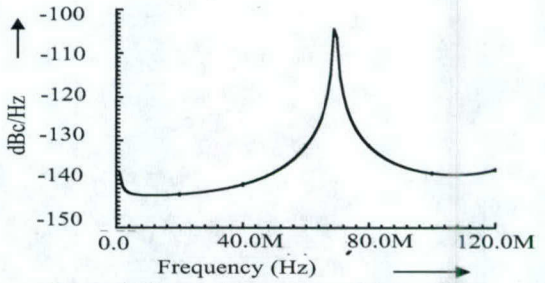


Figure 6. Phase noise spectrum of the oscillator.

The overall performance specifications achieved by the oscillator readout circuit are summarized in Table 1. The pixel size in the designed infrared focal plane array (FPA) is 50 μm x 35 μm. It is possible to achieve a square pixel of 30 μm x 30 μm in the final design by reducing the size of the retention structures for the detector platform. In the actual chip implementation, each oscillator also has an output buffer to prevent the bonding-pad capacitance from loading the oscillator circuit.

Table 1. Oscillator readout circuit performance specifications.

Oscillation frequency	79 MHz
Peak-peak oscillation amplitude	250 mV
Bias current	36 μA
Supply voltage	2.5 V
Sensitivity of oscillation frequency to	
Change in R_d	200 KHz for ΔR_d of 1 KΩ
Change in V_{dd}	0.56% for a ΔV_{dd} of 1%
Change in ambient circuit temperature	0.36% for a change of 1^0C
Phase noise	-104 dBc/Hz @ 1 KHz offset
Output noise	3.96 μv/sqrt (Hz)
Design process	TSMC 0.25 μm
Oscillator chip area	16 μm X 18 μm
Bias and switching circuit chip area	39 μm^2
Ambient circuit temperature	27 ^{0}C

5. CONCLUSIONS

A readout circuit that fully supports the low thermal conduction loss, high sensitivity objective of the levitated infrared sensor has been presented. From Eqn. (8), we know that the oscillation frequency has an inverse square root dependence on the detector resistance.

This circuit can be used effectively to measure changes in the detector resistance due to changes in the incident infrared power by monitoring the corresponding output frequency of the oscillator or in other words, by counting

the number of output pulses observed during a specified readout time. Future work involves laboratory testing of the fabricated integrated readout electronics along with the array addressing modules to verify simulation results. Further research will also endeavor to reduce the sensitivity of the readout circuit to ambient temperature fluctuations and achieve better phase noise response.

REFERENCES

[1] M. L. Reed, T. N. Blalock, *Levitated Infrared Sensor Apparatus and Method of Using the Same*, US patent applied for, February 24, 2001; International patent applied for, February 26, 2001.

[2] Ulf Ringh, Christer Jansson, Christer Svensson, Kevin Liddiard, CMOS analog to digital conversion for uncooled bolometer infrared detector arrays, *SPIE, 2474*.

[3] Behzad Razavi, *Design of analog CMOS integrated circuits* (McGraw-Hill, 2000).

[4] Franco Maloberti, *Analog Design for CMOS VLSI systems* (Kluwer Academic Publishers, 2001).

[5] Ali Hajimiri, Thomas H. Lee, *The design of low noise oscillators* (Kluwer Publications, 1999).

[6] Algie L. Lance, Wendell D. Seal, Frederick Labaar, Phase noise and AM Noise Measurements in the Frequency Domain, *Infrared and Millimeter Waves, 11,* 1984.